LETTER

Air-Stable Ambipolar Field-Effect Transistors and Complementary Logic Circuits from Solution-Processed n/p Polymer Heterojunctions

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ABSTRACT We demonstrate the use of n/p polymer/polymer heterojunctions deposited by sequential solution processing to fabricate ambipolar field-effect transistors and complementary logic circuits. Electron and hole mobilities in the transistors were ~0.001−0.01 $cm^2/(V\ s)$ in air without encapsulation. Complementary circuits integrating multiple ambipolar transistors into NOT, NAND, and NOR gates were fabricated and shown to exhibit sharp signal switching with a high voltage gain.

KEYWORDS: polymer/polymer heterojunction • organic/organic interface • ambipolar charge transport • organic field-effect transistor • complementary logic circuit

INTRODUCTION

Ambipolar organic field-effect transistors (OFETs) have been of great interest for improving circuit performance while reducing complexity of the fabrication because of their multifunctional operation (1−17). Ambipolar OFETs can be implemented in complementary circuits without patterning of the p- and n-type semiconductors. Since the first demonstration of ambipolar charge transport in a bilayer OFET of small-molecule semiconductors (2), ambipolar OFETs have been realized by using various approaches, including heterojunctions (bilayers) (3−7), blends (bulk heterojunctions) (8−10), and single-component organic semiconductors (8, 11−17). An important advantage of the bilayer heterojunction approach is that semiconductor channels are well-defined in separate layers with inherent motifs of molecular packing, making full use of the channel area for charge transport. It may also be possible to embed light-emitting devices, lateral heterojunction diodes, and solar cells into the circuits at the same time if appropriate materials are selected (5, 18−20). However, most heterojunction OFETs studied to date are based on thermally-evaporated small molecules (2−5) or externally-transferred films of polymers, which add additional steps in the fabrication process (6, 7). Making ambipolar OFETs and their complementary circuits from solution-processed n/p polymer/polymer heterojunctions is highly attractive but it remains challenging to achieve because of the difficulty of finding polymer semiconductors with mutually exclusive solubility.

In this report, we demonstrate the fabrication of air-stable ambipolar OFETs based on n/p polymer/polymer heterojunctions and their applications in complementary logic gates, including NOT, NAND and NOR circuits. The n/p polymer semiconductor heterojunctions were processed by sequential spin coating from solutions without film transfer and lamination. Ground-state charge-transfer at the n/p polymer/polymer heterojunctions was not observed by absorption spectroscopy. Ambipolar charge transport in the n/p heterojunctions had electron and hole mobilities of ~0.001−0.01 $cm^2/(V\ s)$, which are similar to those in the parent single-layer OFETs. Ability to prepare well-defined n/p polymer/polymer heterojunctions opens up many new options in the study of device physics and in applications ranging from solar cells and diodes to ambipolar OFETs and logic gates.

EXPERIMENTAL METHODS

The n- and p-type polymer semiconductors and device geometries used in this study are shown in Figure 1. Ladder-type poly(benzobisimidazo-benzophenanthroline) (BBL) was selected as the n-channel layer because it has a high electron mobility ($\mu_e \approx 0.03-0.1\ cm^2/(V\ s)$) and good durability in air (21). Its highest occupied and lowest unoccupied molecular orbitals, HOMO and LUMO levels, are −5.9 and −4.0 eV, respectively (19). The carrier mobility of BBL is strongly dependent on the molecular weight or intrinsic viscosity (22, 23), and the BBL sample used in this study has an intrinsic viscosity of 7.0 dL/g in methanesulfonic acid (MSA) at 30 °C and a typical electron mobility of ~0.001−0.002 $cm^2/(V\ s)$ in air (9, 10). For the p-channel layers, either regioregular poly(3-hexylthiophene) (P3HT) (24, 25), poly(benzobisthiazole-*alt*-3-octylquarterthiophene) (PBTOT) (26), or poly(thiazolothiazole) (PSOTT) was used. These p-channel materials have HOMO levels of −4.9 to −5.2 eV, close to the work function of gold electrodes (~5.1 eV), and LUMO levels of −2.7 to −3.3 eV, resulting in unipolar p-channel operation with field-effect hole mobilities of ~0.01−0.1 $cm^2/(V\ s)$ (12, 24−26).

OFETs with bottom-contact and bottom-gate geometry were made on a heavily *n*-doped silicon wafer with a 200 nm thick

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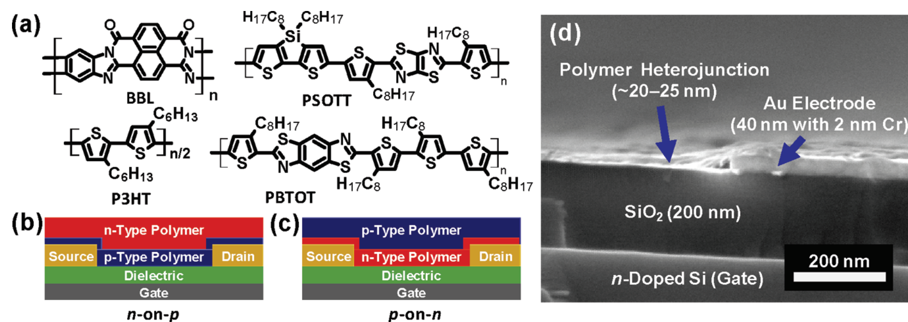

FIGURE 1. (a) Molecular structures of the n-channel (BBL) and p-channel polymer semiconductors (P3HT, PBTOT, and PSOTT). (b, c) Schematics of ambipolar field-effect transistors based on n/p polymer heterojunctions: (b) n-on-p and (c) p-on-n bilayers. (d) Cross-sectional scanning electron microscope image of a transistor based on BBL-on-PBTOT heterojunction.

thermal oxide as the gate electrode and a dielectric layer (capacitance $C_{ox} = 17$ nF/cm^2). Transistor channels with widths (W) of 800−5000 μm and lengths (L) of 40−100 μm (W/L=10, 20, or 50) were defined by photolithographic patterning of gold source-drain electrodes (40 nm thick) with a thin chromium adhesive layer (2 nm) on a substrate. The polymer/polymer semiconductor heterojunctions were deposited by successive spin-coating from solutions in air, forming either n-on-p or p-on-n structures (Figure 1b,c). The p-type polymer layer was spin-coated from solutions in 1,2-dichlorobenzene (P3HT) or 1,2,4-trichlorobenzene (PBTOT and PSOTT). In the case of n-on-p heterojunctions, a very thin film (<10 nm) of the p-type polymer was coated on an OFET substrate modified by octyltrichlorosilane (OTS8). BBL solution in MSA was then spun onto the p-layer, and immediately washed a few times with methanol, water, and/or dimethylsulfoxide to remove the acid solvent. The removal of the acid was continued until the washing medium became neutral pH. The imine-nitrogen in the PBTOT and PSOTT backbones facilitates good wetting of the BBL solution on the p-type layer. However, attempts to prepare BBL-on-P3HT heterojunctions were not successful, because BBL solution did not wet films of P3HT whose surface is highly hydrophobic by virtue of the high density hexyl side chains. Instead, P3HT-on-BBL heterojunctions were used on a substrate without OTS8 modification. The n-on-p and p-on-n bilayer devices were dried in vacuum at room temperature, and then annealed at 140−200 °C for 10 min in nitrogen to remove trace of solvents and to improve molecular ordering. A clean glass substrate was sequentially coated with the p- and n-polymers to study the thin film UV/Vis absorption spectra, with ~5−20 nm thick p-type polymer and/or ~60−80 nm thick BBL. Scanning electron microscope (SEM) imaging was done by using a FEI Sirion SEM with an accelerating voltage of 5 kV.

Electrical testing of devices was carried out by using a HP4145B semiconductor parameter analyzer under nitrogen or a Keithley 4200 semiconductor characterization system in ambient air. Field-effect mobilities were calculated using an equation for saturation region (1): $I_{ds} = \mu W C_{ox}(V_{gs} - V_t)^2/2L$. We used the plots of $|I_{ds}|^{1/2}$ versus V_{gs} with appropriate biases, where the device shows the current saturation in output curves (i.e. large, positive V_{gs} and V_{ds} for calculation of μ_e, and negative biases for μ_h) (16). Because the opposite type of charge carriers can be involved in the operation under certain voltage biases (27), inappropriate selection of data may cause an over-estimation of carrier mobilities. The capacitance of the 200 nm thick SiO_2 (17 nF/cm^2) was used in the calculation of mobilities in both upper and lower layers of the channel.

RESULTS AND DISCUSSION

Well-defined n/p heterojunctions of the polymers in Figure 1 can be sequentially prepared because BBL is soluble in MSA but not in chlorinated aromatic solvents whereas

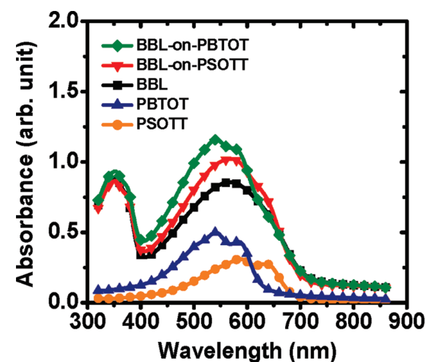

FIGURE 2. Absorption spectra of thin films of BBL (black square), PSOTT (orange circle), and PBTOT (blue upward triangle), and heterojunctions of BBL-on-PSOTT (red downward triangle) and BBL-on-PBTOT (green diamond).

P3HT, PBTOT, and PSOTT are soluble in the latter solvents. During the coating process, no evidence of dewetting of polymeric thin film was observed (Figure S1). Figure 2 shows UV/Vis absorption spectra of thin films of the polymer semiconductors and their bilayered heterojunctions. The absorption spectra of the heterojunctions are simple superposition of the spectra of the component polymers, showing that the heterojunctions were formed from sequential deposition without degradation and that there is no evidence of ground-state charge-transfer at the heterojunctions. The n/p polymer/polymer heterojunctions were spatially not well-resolved in SEM images (Figure 1d) due to the very thin films (≤25 nm) and low contrast between polymer semiconductors. The n/p bilayer heterojunctions offer the potential to effectively use the full channel area in OFETs, allowing the achievement of electron and hole mobilities close to those of the component polymer semiconductors (see below).

Figure 3 shows the electrical characteristics of the OFETs from the *n/p* polymer heterojunctions. Clear $I-V$ characteristics of linear and saturation regions at high V_{gs} and superlinear current increase of typical ambipolar OFETs at low V_{gs} were observed in the output curves (Figure 3a−c) (1), confirming the formation of channels for holes and electrons with well-defined n/p heterojunctions following sequential spin coating. Both electron mobility (μ_e) and hole mobility (μ_h) of n-on-p devices are in the range of ~1×10^{-3} to 1×10^{-2} cm^2/(V s). The similarity of mobilities to those of single-layer OFETs comes from the fact that charge transport occurs in thin conduction sheet defined by the channel

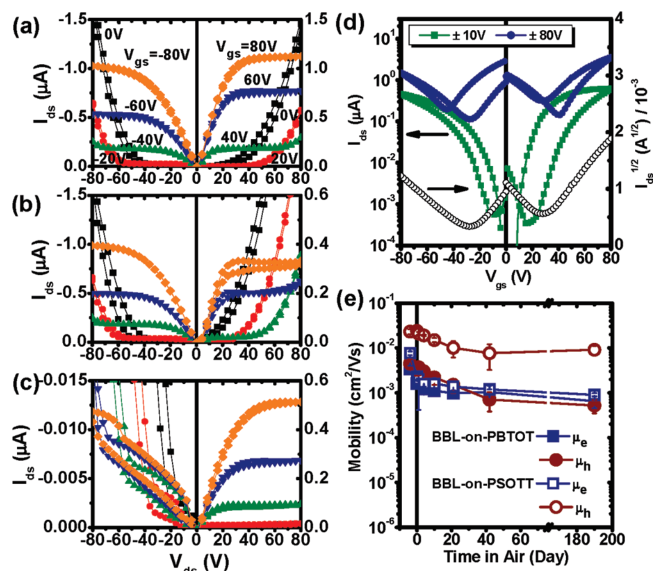

FIGURE 3. (a−c) Output characteristics (plots of I_{ds} vs V_{ds} at different V_{gs}) of n/p bilayer heterojunction transistors: (a) BBL-on-PBTOT, (b) BBL-on-PSOTT, and (c) P3HT-on-BBL. The output curves clearly show the modulation and saturation of current (I_{ds}) under different gate voltage (V_{gs}). Superlinear increase of current under high V_{ds} and low V_{gs} is typical for ambipolar field-effect transistors. (d) Transfer curves (plots of I_{ds} and $I_{ds}^{1/2}$ vs V_{gs} at fixed V_{ds}) of a BBL-on-PBTOT bilayer transistor. The transfer curves under different V_{ds} can be found in Figure S2. Charge-carrier mobilities were calculated from the slope of $I_{ds}^{1/2}$ at $V_{ds} = \pm 80$ V. (e) Hole and electron mobilities in the BBL-on-PBTOT and BBL-on-PSOTT transistors as a function of time in air. Data points before day 0 represent the mobilities in inert conditions.

dimensions (W and L). Average electron and hole mobilities in BBL-on-PBTOT are 0.0051 cm^2/(V s) and 0.0078 cm^2/(V s), respectively. BBL-on-PSOTT showed a higher average hole mobility of 0.012 cm^2/(V s), whereas the observed average electron mobility was 0.0058 cm^2/(V s). The on/off ratios of the OFETs are $\sim 1 \times 10^3$ with low V_{ds} (± 10 V), whereas the ratios become ~ 10 when $V_{ds} = \pm 80$ V (Figure 3d). Average threshold voltages for n- and p-channel modes are 4.3 V and −10.1 V in BBL-on-PBTOT, and 19.8 V and 5.9 V in BBL-on-PSOTT, respectively. In P3HT-on-BBL devices, the mobilities are rather low and asymmetric compared to the other systems (Figure 3c). The electron mobility of 0.002 cm^2/(V s) is similar to the previously reported values of BBL on SiO_2 (9, 10). It is interesting that μ_e in n-on-p devices is generally higher than in p-on-n, despite potential electron-injection barriers of n-on-p devices. The higher μ_e might come from the absence of electron-trapping silol groups (12) covered by OTS8 and *p*-type polymers. The very low mobility of holes ($\sim 1 \times 10^{-5}$ cm^2/(V s)) in P3HT-on-BBL devices can be attributed to the fact that the underlying BBL layer is relatively thick (∼20−30 nm) and rough ($R_q \approx 5$ nm). A thick underlying layer can act as a barrier for hole injection (2), and a rough interface scatters the charge carriers in the p-channel (28), resulting in the much lower hole mobility in P3HT. It should be noted that corrections for contact resistance and capacitance change caused by the presence of a bottom-channel layer have not been made in the calculation of the mobility of the top channel.

Field-effect mobilities of electrons and holes in the n/p heterojunction OFETs in air have been tracked for more than 6 months (Figure 3e), demonstrating good stability. The OFET mobilities were initially measured in nitrogen and then stored and periodically tested in air. The hole mobilities in PBTOT and PSOTT p-layers decreased from 0.0045 and 0.023 cm^2/(V s) to 0.0007 and 0.0077 cm^2/(V s), respectively, after 42 days stored and tested in air. The mobilities measured after 190 days in air were 0.0005 cm^2/(V s) and 0.0093 cm^2/(V s), respectively. Although in general p-type semiconductors are energetically less susceptible to external dopants that result in degradation of the carrier mobility than n-type materials, very thin layer (≤ 10 nm) of electrically active p-channel may be vulnerable to dopants due to the lack of kinetic barrier for diffusion of oxidant molecules to the charge accumulation channel (29). On the other hand, the electron mobilities in both systems were initially dropped from ∼0.003−0.008 cm^2/(V s) to ∼0.001−0.002 cm^2/(V s) and stabilized with little fluctuations over time.

Digital logic circuits, which perform a logic calculation of binary information (represented by 0 and 1), have played an essential role in development of current information technology. The circuits are fabricated by integration of multiple field-effect transistors. Sharp signal switching of the circuits can be obtained from complementary circuits that consist of p- and n-type transistors or ambipolar transistors (1, 16). Each transistor is selectively turned on and off based on the voltages at the terminal electrodes, inducing current flow through a certain pathway of the circuit and resulting in the targeted output voltage, which is close to either the supplied voltage (V_{dd}; represents signal 1) or ground (represents signal 0), of the logic operation. For example, the input signal is inverted after NOT gate operation (from 0 to 1, or from 1 to 0). The output signal of NAND gate is 0 only when two input signals are 1; otherwise the output is 1. The NOR operation results in 1 only when the input signals are both 0. Complementary NOT gate requires one n-channel and one p-channel transistors, and complementary NAND and NOR gates require two n-channel and two p-channel transistors each. Logic gates based on ambipolar transistors require one type of transistor, although the total number of transistors is the same as circuits with unipolar transistors (Figure 4a).

Complementary logic gates, including NOT, NAND, and NOR circuits, based on the integrated ambipolar OFETs exhibited sharp switching as shown in Figure 4. Circuit diagrams of an inverter (NOT-gate) consisting of two transistors, and two-input NAND and NOR circuits with four transistors each are shown in Figure 4a. The circuits consist of identical ambipolar OFETs from BBL-on-PBTOT n/p heterojunctions with the same geometric factors ($C_{ox} = 17$ nF/cm^2, $W = 5000$ μm, and $L = 100$ μm). Voltage transfer characteristics of the inverter showed sharp switching, which is typical for complementary circuits (1), with a high gain ($-dV_{out}/dV_{in}$) of 16−18 reproducibly obtained at $V_{dd} = \pm 80$ V (Figure 4b). The output voltage offsets from V_{dd} and 0 V are also typical for logic circuits based on ambipolar transistors (1, 16). Some degree of hysteresis is likely due to the

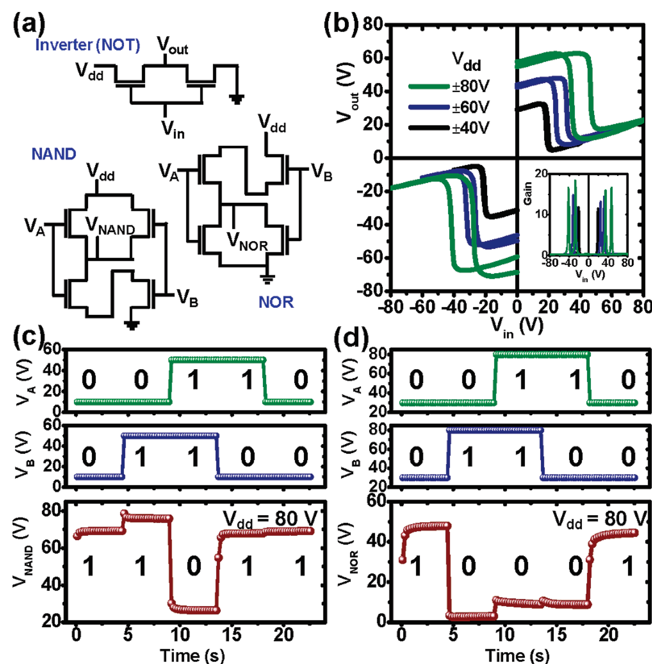

FIGURE 4. (a) Circuit diagrams of a complementary inverter, and NAND and NOR logic gates. (b) Voltage transfer characteristics of an inverter. (c, d) Output voltages of complementary logic gates and the truth tables with corresponding input voltages V_A and V_B: (c) NAND and (d) NOR gates. The transistors in the circuits are based on BBL-on-PBTOT heterojunctions.

threshold voltage difference of n- and p-channel modes in the individual OFETs.

In the logic circuits of NAND and NOR gates, good switching characteristics were also observed, as shown in the output voltages plotted with the corresponding input voltages V_A and V_B (Figure 4c,d). High and low voltages at the terminals represent signals 1 and 0, respectively. The truth tables are included in panels c and d in Figure 4 to clarify the logic operations. We note that the NAND gate based on the ambipolar transistors is converted into the NOR gates, and vice versa, by simply swapping terminals of V_{dd} and ground since the constituent transistors are identical. The results demonstrate that ambipolar OFETs can be used for designing and constructing various complementary circuits. Because the ambipolar transistors and circuits are fabricated by simple solution processes, the devices presented here could ultimately be printable and the approach should be applicable to real electronic devices as the technology further develops.

CONCLUSIONS

In conclusion, we have shown that well-defined heterojunctions of n- and p-type polymer semiconductors prepared by solution processing can be used to realize OFETs with good ambipolar charge transport. Ambipolar charge transport with balanced charge-carrier mobilities that are close to those in their component unipolar semiconductors was achieved in air without encapsulation. NOT, NAND, and NOR logic gates based on the ambipolar n/p heterojunction OFETs were also demonstrated with good signal switching. These results suggest that high-performance complex complementary circuits could be achieved via solution-processed ambipolar polymer OFETs.

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Supporting Information Available: AFM topographic images, detailed transfer characteristics, and air-stability of the devices (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.

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